IN THE SPECIFICATION

Please amend the paragraph on page 1, beginning on line 4, as follows.

The embodiments of the present invention ~~relates~~ relate to data transfer interface technology in a data network, and more particularly, relates to a link level packet flow control mechanism utilized to prevent loss of data packets due to receive buffer overflow at either end of a transmission link (a full duplex transmission path between any two network fabric nodes, such as channel adapters installed at host systems) in such a data network.

Please amend the paragraph on page 5, beginning on line 2, as follows.

The embodiments of the present invention [[is]] are applicable for use with all types of data networks, I/O hardware adapters and chipsets, including follow-on chip designs which link together end stations such as computers, servers, peripherals, storage subsystems, and communication devices for data communications. Examples of such data networks may include a local area network (LAN), a wide area network (WAN), a campus area network (CAN), a metropolitan area network (MAN), a global area network (GAN), a wireless personal area network (WPAN), and a system area network (SAN), including newly developed computer networks using Next Generation I/O (NGIO), Future I/O (FIO), InfiniBandTM, Server Net and those networks including channel-based, switched fabric architectures which may become available as computer technology advances to provide scalable performance. LAN systems may include Ethernet, FDDI (Fiber Distributed Data Interface) Token Ring LAN, Asynchronous Transfer Mode (ATM) LAN, Fiber Channel, and Wireless LAN. However, for the sake of simplicity, discussions will concentrate mainly on a host system including one or more hardware fabric adapters for providing physical links for channel connections in a simple data network having several example nodes (e.g., computers, servers and I/O units) interconnected by

corresponding links and switches, although the scope of the present invention is not limited thereto.

Please amend the paragraph on page 9, beginning on line 15, as follows.

Host channel adapter (HCA) 120 may be used to provide an interface between a memory controller (not shown) of the host system 130 (e.g., servers) and a switched fabric 100' via high speed serial NGIO/InfiniBandTM links. Similarly, target channel adapters (TCA) 140 and 160 may be used to provide an interface between the multi-stage switched fabric 100' and an I/O controller (e.g., storage and networking devices) of either a second network 150 or an I/O unit 170 via high speed serial NGIO/InfiniBandTM links. Separately, another target channel adapter (TCA) 180 may be used to provide an interface between a memory controller (not shown) of the remote system 190 and the switched fabric 100' via high speed serial NGIO/InfiniBandTM links. Both the host channel adapter (HCA) and the target channel adapter (TCA) may be broadly considered as fabric adapters provided to interface either the host system 130 or any one of the remote systems 150, 170 and 190 to the switched fabric 100', and may be implemented in compliance with "Next Generation I/O Link Architecture Specification: HCA Specification, Revision 1.0" and the "InfiniBandTM Architecture Specification" for enabling the endpoints (nodes) to communicate to each other over an NGIO/InfiniBandTM channel(s). However, NGIO/InfiniBandTM is merely one example embodiment or implementation of the present invention, and the invention is not limited thereto. Rather, the embodiments of the present invention may be applicable to a wide variety of any number of data networks, hosts and I/O units. For example, practice of the embodiments of the invention may also be made with Future Input/Output (FIO). FIO specifications have not yet been released, owing to subsequent merger agreement of NGIO and FIO factions combine efforts on InfiniBandTM Architecture specifications as set forth by the InfiniBand Trade Association (formed August 27, 1999) having an Internet address of "http://www.InfiniBandta.org."

Please amend the paragraph on page 32, beginning on line 19, as follows.

While there have been illustrated and described what are considered to be exemplary embodiments of the present invention, it will be understood by those skilled in the art and as technology develops that various changes and modifications may be made, and equivalents may be substituted for elements thereof without departing from the true scope of the present invention. For example, the computer network as shown in FIGs. 1-2 may be configured differently or employ some or different components than those illustrated. Such computer network may include a local area network (LAN), a wide area network (WAN), a campus area network (CAN), a metropolitan area network (MAN), a global area network (GAN) and a system area network (SAN), including newly developed computer networks using Next Generation I/O (NGIO) and Future I/O (FIO) and Server Net and those networks which may become available as computer technology advances in the future. LAN system may include Ethernet, FDDI (Fiber Distributed Data Interface) Token Ring LAN, Asynchronous Transfer Mode (ATM) LAN, Fiber Channel, and Wireless LAN. In addition, the flow control mechanism shown in FIGs. 7-9 may be configured differently or employ some or different components than those illustrated without changing the basic function of the invention. For example, different combinations of logic gates such as AND, OR, NOR, NAND etc. may be used to implement per VL Link Packet Scheduler 720 shown in FIG. 9. Many modifications may be made to adapt the teachings of the embodiments of the present invention to a particular situation without departing from the scope thereof. Therefore, it is intended that the embodiments of the present invention not be limited to the various exemplary embodiments disclosed, but that the embodiments of the present invention ~~includes~~ include all embodiments falling within the scope of the appended claims.